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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,823	10/17/2003	Sam Yang	303.660US7	2377

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,823	YANG ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-10,12,13,15-19,23-27,29,30 and 32-35* is/are rejected.

7)☒ Claim(s) *3-5,11,14,20-22,28 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 9 recites the limitation "the metal oxide dielectric layer" on line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al.. As to claim 1, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14); a top electrode (19); a dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of memory

cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al.. The motivation for doing so would have been to operate the array of cells in a useful manner. Therefore, it would have been obvious to combine Basceri et al. with Agarwal et al. to obtain the invention as specified in claim 1.

As to claim 2, Agarwal et al., (col. 5, lines 23-24) discloses that the metal oxynitride barrier layer comprises tantalum oxynitride.

As to claim 6, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of a metal nitride.

As to claim 7, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of tungsten nitride.

As to claim 8, Agarwal et al., (col. 4, lines 35-36) discloses that the dielectric layer may be made from tantalum oxide, strontium titanate, or barium strontium titanate.

As to claim 9, Agarwal et al., (col. 4, line 35) discloses that the dielectric layer may be comprised of tantalum oxide.

Claims 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al. and further in view of Deng et al.. As to claim 10, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14); a top electrode (19); a dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory

device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of memory cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. Deng et al. discloses the use of group VI metals (which includes tungsten) in the formation of a metal (tungsten) oxynitride. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al. and the barrier layer of Deng et al.. The motivation for doing so would have been to operate the array of cells in a useful manner, and with a less expensive material, tungsten, rather than, for example, tantalum. Therefore, it would have been obvious to combine Basceri et al. and Deng et al. with Agarwal et al. to obtain the invention as specified in claim 10.

As to claim 12, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of a metal nitride.

As to claim 13, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of tungsten nitride.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al. and further in view of Deng et al.. As to claim 15, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14); a top electrode (19); a metal oxide dielectric layer (16)(col. 4, line 35) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of memory cells (402). Basceri et al., Figure 4, also

discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. Deng et al. discloses the use of group VI metals (which includes tungsten) in the formation of a metal (tungsten) oxynitride. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al. and the barrier layer of Deng et al.. The motivation for doing so would have been to operate the array of cells in a useful manner, and with a less expensive material, tungsten, rather than, for example, tantalum. Therefore, it would have been obvious to combine Basceri et al. and Deng et al. with Agarwal et al. to obtain the invention as specified in claim 15.

As to claim 16, Agarwal et al., (col. 4, line 35) discloses that the metal oxide layer comprises tantalum oxide.

As to claim 17, Agarwal et al., (col. 4, line 22) discloses that the bottom and top electrodes may comprise tungsten nitride.

Claims 18, 19 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al.. As to claim 18, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14), which may have a metal component (col. 4, lines 20-22); a top electrode (19), which may have a metal component (col. 4, lines 20-22 and col. 5, lines 37-39); a dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of memory cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the

array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al.. The motivation for doing so would have been to operate the array of cells in a useful manner. Therefore, it would have been obvious to combine Basceri et al. with Agarwal et al. to obtain the invention as specified in claim 18.

As to claim 19, Agarwal et al., (col. 5, lines 23-24) discloses that the metal oxynitride barrier layer comprises tantalum oxynitride.

As to claim 23, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of a metal nitride.

As to claim 24, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of tungsten nitride.

As to claim 25, Agarwal et al., (col. 4, lines 35-36) discloses that the dielectric layer may be made from tantalum oxide, strontium titanate, or barium strontium titanate.

As to claim 26, Agarwal et al., (col. 4, line 35) discloses that the dielectric layer may be comprised of tantalum oxide.

Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al. and further in view of Deng et al.. As to claim 27, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14), which may have a metal component (col. 4, lines 20-22); a top electrode (19), which may have a metal component (col. 4, lines 20-22 and col. 5, lines 37-39); a dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of

leads; and at least one memory device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of memory cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. Deng et al. discloses the use of group VI metals (which includes tungsten) in the formation of a metal (tungsten) oxynitride. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al. and the barrier layer of Deng et al.. The motivation for doing so would have been to operate the array of cells in a useful manner, and with a less expensive material, tungsten, rather than, for example, tantalum. Therefore, it would have been obvious to combine Basceri et al. and Deng et al. with Agarwal et al. to obtain the invention as specified in claim 27.

As to claim 29, Agarwal et al., (col. 4, line 22) discloses that the lower electrode may be comprised of a metal nitride.

Claims 30, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al. and further in view of Deng et al.. As to claim 30, Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14), which may have a metal component (col. 4, lines 20-22); a top electrode (19), which may have a metal component (col. 4, lines 20-22 and col. 5, lines 37-39); a metal oxide dielectric layer (16)(col. 4, line 35) dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al., (col. 4, line 22) also discloses that the lower electrode may be comprised of a metal nitride. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory device (610) contained on the support and coupled to the command link, wherein the at least one memory device comprises an array of

memory cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. Deng et al. discloses the use of group VI metals (which includes tungsten) in the formation of a metal (tungsten) oxynitride. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al. and the barrier layer of Deng et al.. The motivation for doing so would have been to operate the array of cells in a useful manner, and with a less expensive material, tungsten, rather than, for example, tantalum. Therefore, it would have been obvious to combine Basceri et al. and Deng et al. with Agarwal et al. to obtain the invention as specified in claim 30.

As to claim 32, Agarwal et al., (col. 4, line 35) discloses that the dielectric layer may be comprised of tantalum oxide.

As to claim 33, Agarwal et al., (col. 4, line 22) discloses that the lower and upper electrodes may be comprised of tungsten nitride.

Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. in view of Basceri et al. and further in view of Deng et al Agarwal et al., Figure 1C, discloses a memory cell with a capacitor, the capacitor comprising: a bottom electrode (14), which may have a metal component (col. 4, lines 20-22); a top electrode (19), which may have a metal component (col. 4, lines 20-22 and col. 5, lines 37-39); a metal oxide dielectric layer (16)(col. 4, line 35) dielectric layer (16) interposed between the bottom electrode and the top electrode; and one metal oxynitride barrier layer (18a)(col. 5, lines 23-24), wherein the metal oxynitride barrier layer is interposed between the dielectric layer and the upper electrode. Agarwal et al., (col. 4, line 22) also discloses that the lower electrode may be comprised of a metal nitride. Agarwal et al. does not disclose expressly the cell formed in an array, or necessary support circuitry. Basceri et al., Figures 4, 6 and 7, discloses a memory module, comprising: a support (600); a plurality of leads (612) extending from the support; a command link (720) coupled to at least one of the plurality of leads; a plurality of data links (730), wherein each data link is coupled to at least one of the plurality of leads; and at least one memory device (610) contained on the support and

coupled to the command link, wherein the at least one memory device comprises an array of memory cells (402). Basceri et al., Figure 4, also discloses a row access circuit (406) coupled to the array of memory cells; a column access circuit (408) coupled to the array of memory cells, and an address decoder circuit (404) coupled to the row access circuit and the column access circuit. Deng et al. discloses the use of group VI metals (which includes tungsten) in the formation of a metal (tungsten) oxynitride. At the time of invention, it would have been transparently obvious to a person of ordinary skill in the art to form the cell of Agarwal et al. with the necessary support circuitry of Basceri et al. and the barrier layer of Deng et al.. The motivation for doing so would have been to operate the array of cells in a useful manner, and with a less expensive material, tungsten, rather than, for example, tantalum. Therefore, it would have been obvious to combine Basceri et al. and Deng et al. with Agarwal et al. to obtain the invention as specified in claim 34.

As to claim 35, Agarwal et al., (col. 4, line 22) discloses that the upper electrode may be comprised of tungsten nitride.

Double Patenting

Claim 14 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 11. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

Claims 3, 4, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed stoichiometric ranges of the metal oxynitrides with the claimed metal species.

Claims 5, 11, 22, 28 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses a tungsten oxynitride barrier layer with the claimed stoichiometric ranges.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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srw
January 26, 2005